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DRAM MODULE

1 MEG, 2 MEG x 32

4, 8 MEGABYTE, 5V, FAST PAGE OR EDO PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process.
- Single +5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 48mW standby; 1,824mW active, typical (8MB)
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Multiple $\overline{RAS}$ lines allow x16 or x32 width
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE (FPM) operating mode or Extended Data-Out (EDO) PAGE MODE operating mode

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access (FAST PAGE MODE only) — -7
- Packages
  - 72-pin SIMM — M
  - 72-pin SIMM (gold) — G
- Operating Modes
  - FAST PAGE MODE — Blank
  - EDO PAGE MODE — X

KEY TIMING PARAMETERS

EDO Operating Mode

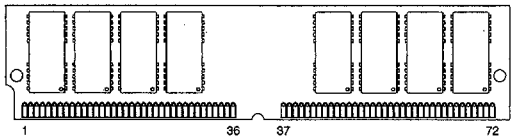
SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-6	110ns	60ns	26ns	30ns	17ns	13ns

FPM Operating Mode

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)

72-Pin SIMM
(DD-3) 1 Meg x 32
(DD-4) 2 Meg x 32



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC*/$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC*/$\overline{RAS3}$	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

*4MB version only

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PART NUMBERS

EDO Operating Mode

PART NUMBER	DESCRIPTION
MT8D132G-xx X	1 Meg x 32, EDO, Gold
MT8D132M-xx X	1 Meg x 32, EDO, Tin/Lead
MT16D232G-xx X	2 Meg x 32, EDO, Gold
MT16D232M-xx X	2 Meg x 32, EDO, Tin/Lead

xx = speed

FPM Operating Mode

PART NUMBER	DESCRIPTION
MT8D132G-xx	1 Meg x 32, Gold
MT8D132M-xx	1 Meg x 32, Tin/Lead
MT16D232G-xx	2 Meg x 32, Gold
MT16D232M-xx	2 Meg x 32, Tin/Lead

xx = speed

GENERAL DESCRIPTION

The MT8D132(X) and MT16D232(X) are randomly accessed 4MB and 8MB solid-state memories organized in a x32 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ goes back HIGH. EDO provides for $\overline{CAS}$ precharge time (^{t}CP) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control provides for pipeline READs.

FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after $\overline{CAS}$ goes HIGH, as long as $\overline{RAS}$ and $\overline{OE}$ are held LOW and $\overline{WE}$ is held HIGH (reference MT4C4007J DRAM data sheet for additional information on EDO functionality).

REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 1,024 combination of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

x16 CONFIGURATION

For x16 applications, the corresponding DQ and $\overline{CAS}$ pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the x16 memory organization.

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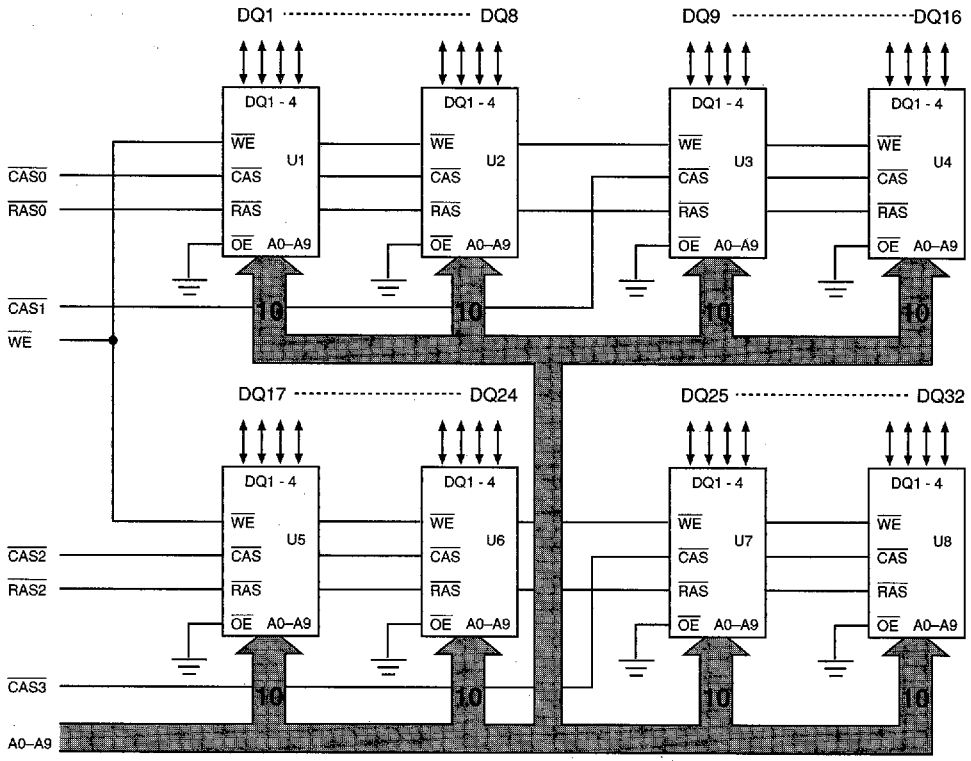
FUNCTIONAL BLOCK DIAGRAM
MT8D132(X) (4MB)



FAST PAGE MODE
U1-U8 = MT4C4001JDJ

EDO PAGE MODE
U1-U8 = MT4C4007JDJ

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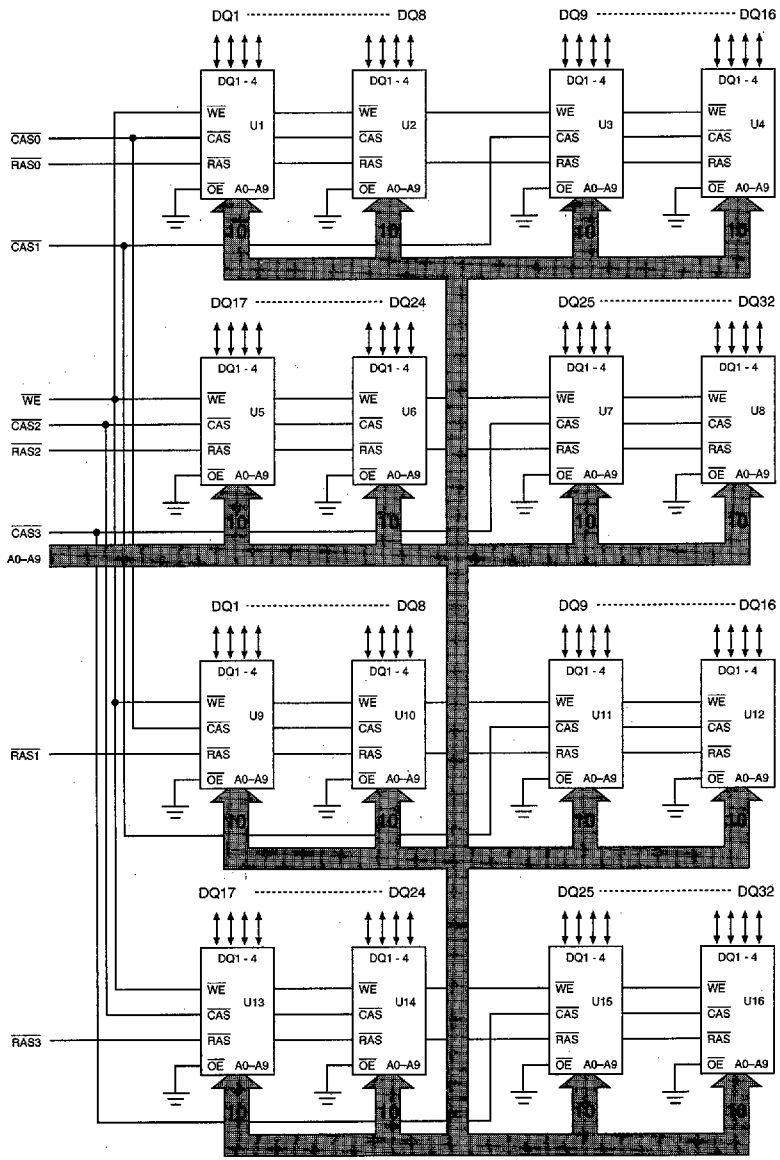
FUNCTIONAL BLOCK DIAGRAM
MT16D232(X) (8MB)



FAST PAGE MODE
U1-U16 = MT4C4001J

EDO PAGE MODE
U1-U16 = MT4C4007JDJ

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TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA-IN/OUT
					^tR	^tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
	Any Cycle (X version)	L	L→H	H	n/a	n/a	Data-Out
EDO/FAST-PAGE-MODE EARLY WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

JEDEC DEFINED PRESENCE-DETECT - MT8D132(X) (4MB)

SYMBOL	PIN #	-6	-7
PRD1	67	Vss	Vss
PRD2	68	Vss	Vss
PRD3	69	NC	Vss
PRD4	70	NC	NC

JEDEC DEFINED PRESENCE-DETECT - MT16D232(X) (8MB)

SYMBOL	PIN #	-6	-7
PRD1	67	NC	NC
PRD2	68	NC	NC
PRD3	69	NC	Vss
PRD4	70	NC	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	II1	-8	8	µA	
Any input 0V ≤ VIN ≤ Vcc +1.0V	A0-A9, $\overline{WE}$	II2	-32	32	µA	25
(All other pins not under test = 0V)	$\overline{RAS0}$-$\overline{RAS3}$	II3	-8	8	µA	25
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ32	IOZ	-20	20	µA	25
OUTPUT LEVELS		VOH	2.4		V	
High Voltage (IOUT = -5mA)		VOL		0.4	V	
Low Voltage (IOUT = 4.2mA)						

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	4MB 8MB	16 32	16 32	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = other inputs = Vcc -0.2V)	ICC2	4MB 8MB	8 16	8 16	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: tRC = tRC [MIN])	ICC3	4MB 8MB	880 896	800 816	mA	2, 24
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, address cycling: tPC = tPC [MIN])	ICC4	4MB 8MB	640 656	560 576	mA	2, 24
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, address cycling: tPC = tPC [MIN])	ICC5 (X only)	4MB 8MB	640 656	— —	mA	2
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = VIH: tRC = tRC [MIN])	ICC6	4MB 8MB	880 896	800 816	mA	2, 24
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: tRC = tRC [MIN])	ICC7	4MB 8MB	880 896	800 816	mA	2, 19

DRAM SIMM

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CAPACITANCE

PARAMETER	SYMBOL	MAX 4MB	MAX 8MB	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	48	95	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}	64	127	pF	17
Input Capacitance: $\overline{RAS0}$-$\overline{RAS3}$	C_{I4}	32	32	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I5}	16	32	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}	10	18	pF	17

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from $\overline{CAS}$	^tCAC		15		20	ns	9
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	18
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	19
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	15
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	12, 23, 26
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	8
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	22
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	14
Read command setup time	^tRCS	0		0		ns	
Refresh period (1,024 cycles)	^tREF		16		16	ms	

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FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (Vcc = +5V ±10%)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{RAS}$ precharge time	t_{RP}	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0		0		ns	
Read command hold time	t_{RRH}	0		0		ns	14
$\overline{RAS}$ hold time	t_{RSH}	15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		ns	
Transition time (rise or fall)	t_T	3	50	3	50	ns	
Write command hold time	t_{WCH}	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	45		55		ns	
$\overline{WE}$ command setup time	t_{WCS}	0		0		ns	
Write command pulse width	t_{WP}	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	t_{WRH}	10		10		ns	
$\overline{WE}$ setup time (CBR REFRESH)	t_{WRP}	10		10		ns	

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column-address	^tAA		30	ns	
Column-address setup to $\overline{CAS}$ precharge during WRITE	^tACH	15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		ns	
Column-address setup time	^tASC	0		ns	
Row-address setup time	^tASR	0		ns	
Access time from $\overline{CAS}$	^tCAC		17	ns	9
Column-address hold time	^tCAH	10		ns	
$\overline{CAS}$ pulse width	^tCAS	13	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		ns	23
Data output hold after $\overline{CAS}$ LOW	^tCOH	5		ns	
$\overline{CAS}$ precharge time	^tCP	10		ns	18
Access time from $\overline{CAS}$ precharge	^tCPA		35	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		ns	
$\overline{CAS}$ hold time	^tCSH	50		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		ns	19
Write command to $\overline{CAS}$ lead time	^tCWL	15		ns	
Data-in hold time	^tDH	9		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		ns	
Data-in setup time	^tDS	0		ns	15
Output buffer turn-off delay	^tOFF	3	15	ns	12, 23, 26
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	26		ns	
Access time from $\overline{RAS}$	^tRAC		60	ns	8
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	ns	22
Row-address hold time	^tRAH	10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	ns	
Random READ or WRITE cycle time	^tRC	110		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		ns	14
Read command setup time	^tRCS	0		ns	
Refresh period (1,024 cycles)	^tREF		16	ms	

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EDO PAGE MODE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{RAS}$ precharge time	t_{RP}	40		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		ns	
Read command hold time	t_{RRH}	0		ns	14
$\overline{RAS}$ hold time	t_{RSH}	15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		ns	
Transition time (rise or fall)	t_T	1.5	50	ns	4, 5
Write command hold time	t_{WCH}	10		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	45		ns	
$\overline{WE}$ command setup time	t_{WCS}	0		ns	
Output disable delay from $\overline{WE}$ ($\overline{CAS}$ HIGH)	t_{WHZ}	3	15	ns	
Write command pulse width	t_{WP}	10		ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ HIGH	t_{WPZ}	10		ns	
$\overline{WE}$ hold time (CBR REFRESH)	t_{WRH}	10		ns	
$\overline{WE}$ setup time (CBR REFRESH)	t_{WRP}	10		ns	

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NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns for FAST PAGE MODE and ^{t}T = 1.5ns for EDO PAGE MODE.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge {}^{t}RCD$ (MAX).
10. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 4.5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U8/U16.
22. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
23. The 3ns minimum is a parameter guaranteed by design.
24. Column-address changed once each cycle.
25. 4MB module values will be half of those shown.
26. For FAST PAGE MODE option, ^{t}OFF is determined by the first $\overline{RAS}$ or $\overline{CAS}$ signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the $\overline{RAS}$ and $\overline{CAS}$ signal to transition HIGH.
27. Applies to both EDO and FAST PAGE MODEs.

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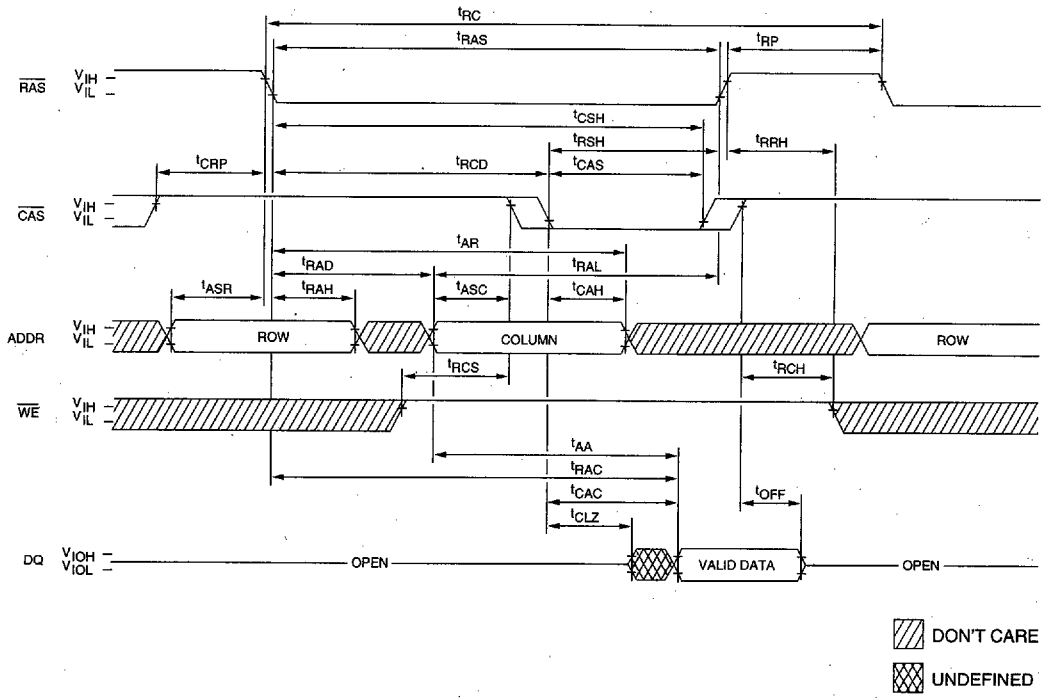
6111549 0013568 500

READ CYCLE
(FAST PAGE MODE Module)



FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	0		0		ns
tCRP	10		10		ns
tCSH	60		70		ns
tOFF	3	15	3	20	ns
tRAC		60		70	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC	110		130		ns
tRCD	20	45	20	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	15		20		ns

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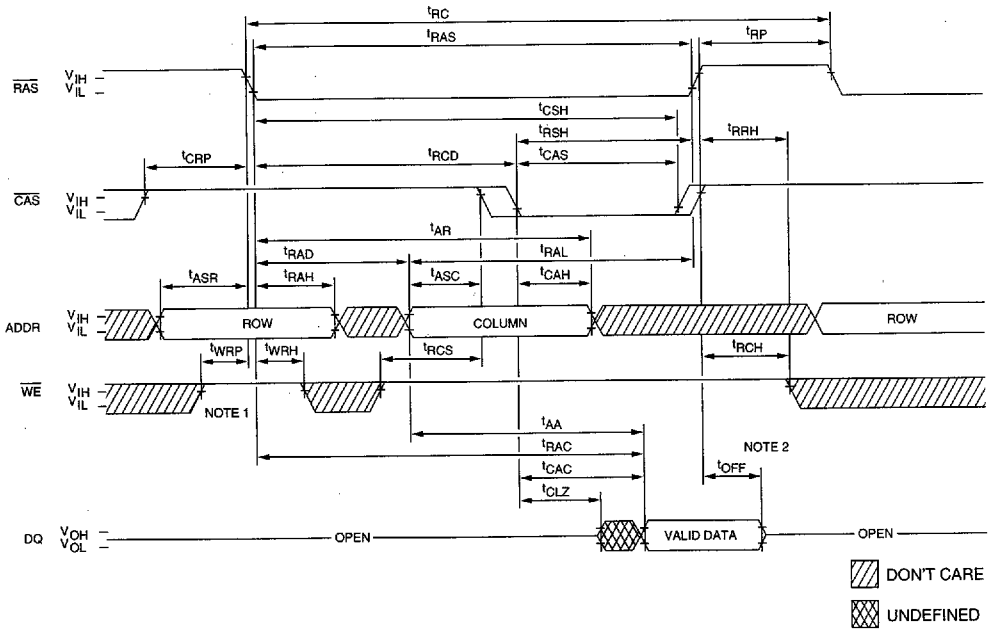
6111549 0013569 447

READ CYCLE
(EDO PAGE MODE Module)



NOTE:
1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

EDO PAGE MODE TIMING PARAMETERS

	-6		
SYM	MIN	MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		17	ns
tCAH	10		ns
tCAS	13	10,000	ns
tCLZ	3		ns
tCRP	10		ns
tCSH	50		ns
tOFF	3	15	ns
tRAC		60	ns
tRAD	15	30	ns

	-6		
SYM	MIN	MAX	UNITS
tRAH	10		ns
tRAL	30		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20	45	ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns
tWRH	10		ns
tWRP	10		ns

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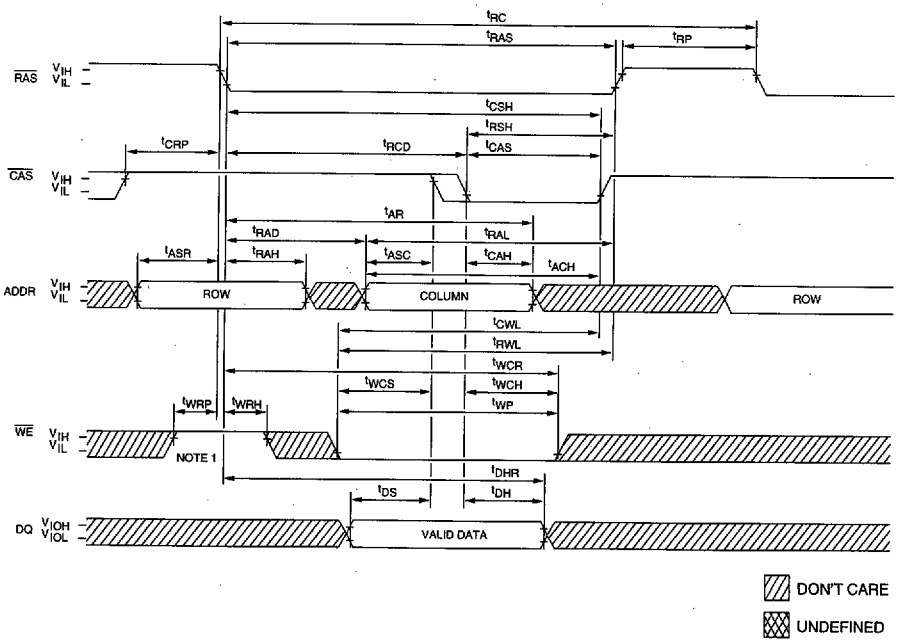
6111549 0013570 169

EARLY WRITE CYCLE [27]



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tACH (EDO)	15		—		ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	10		15		ns
tCAS (FPM)	15	10,000	20	10,000	ns
tCAS (EDO)	13	10,000	—	—	ns
tCRP	10		10		ns
tCSH (FPM)	60		70		ns
tCSH (EDO)	50		—		ns
tCWL	15		20		ns
tDH (FPM)	10		15		ns
tDH (EDO)	9		—		ns
tDHR	45		55		ns
tDS	0		0		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC	110		130		ns
tRCD	20	45	20	50	ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCR	45		55		ns
tWCS	0		0		ns
tWP	10		15		ns
tWRH	10		10		ns
tWRP	10		10		ns

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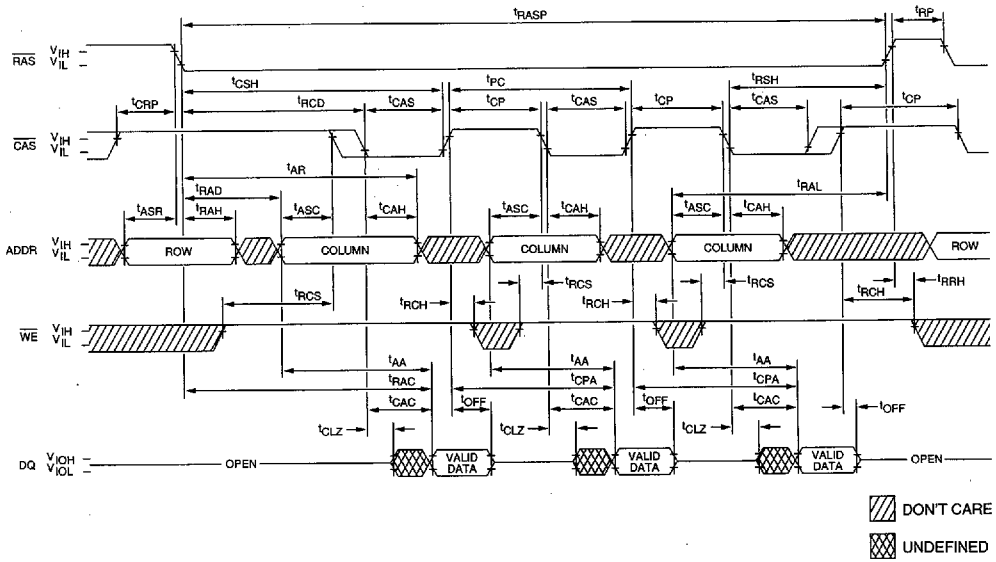
6111549 0013571 0T5

FAST-PAGE-MODE READ CYCLE



FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	0		0		ns
tCP	10		10		ns
tCPA		35		40	ns
tCRP	10		10		ns
tCSH	60		70		ns
tOFF	3	15	3	20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tPC	35		40		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	15		20		ns

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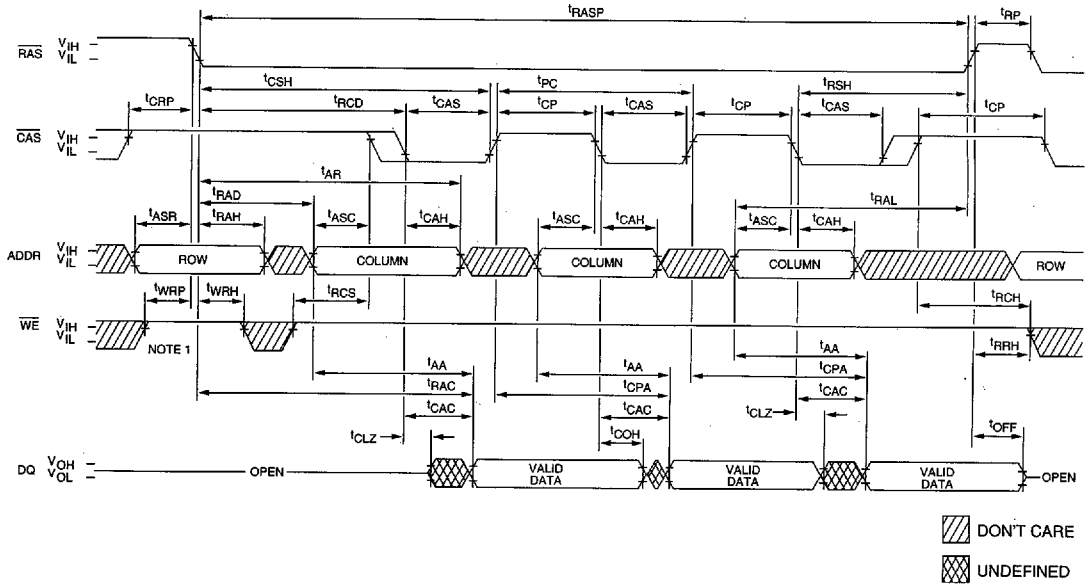
6111549 0013572 T31

EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		
SYM	MIN	MAX	UNITS
^{t}AA		30	ns
^{t}AR	45		ns
^{t}ASC	0		ns
^{t}ASR	0		ns
^{t}CAC		17	ns
^{t}CAH	10		ns
^{t}CAS	13	10,000	ns
^{t}CLZ	3		ns
^{t}COH	5		ns
^{t}CP	10		ns
^{t}CPA		35	ns
^{t}CRP	10		ns
^{t}CSH	50		ns
^{t}OFF	3	15	ns

	-6		
SYM	MIN	MAX	UNITS
^{t}PC	26		ns
^{t}RAC		60	ns
^{t}RAD	15	30	ns
^{t}RAH	10		ns
^{t}RAL	30		ns
^{t}RASP	60	100,000	ns
^{t}RCD	20	45	ns
^{t}RCH	0		ns
^{t}RCS	0		ns
^{t}RP	40		ns
^{t}RRH	0		ns
^{t}RSH	15		ns
^{t}WRH	10		ns
^{t}WRP	10		ns

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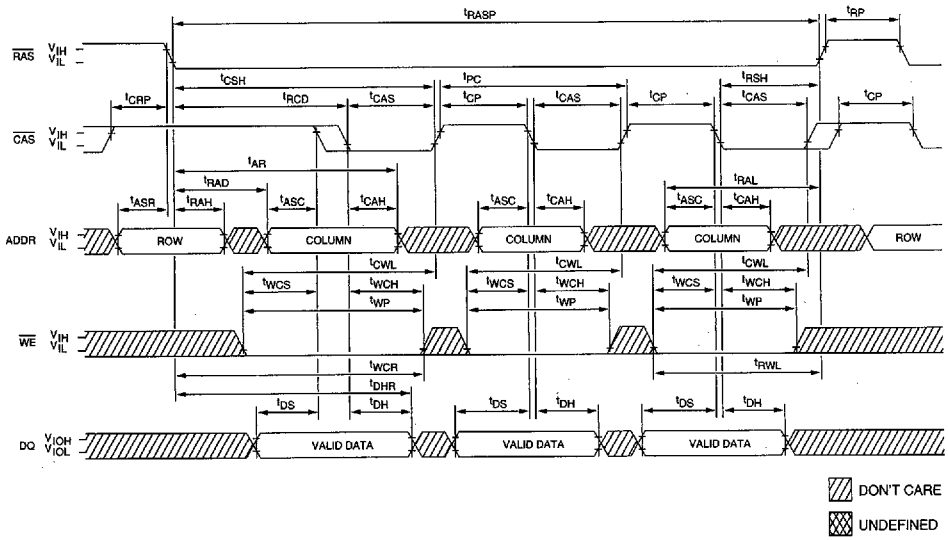
FAST-PAGE-MODE EARLY-WRITE CYCLE



DRAM SIMM

FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCP	10		10		ns
tCRP	10		10		ns
tCSH	60		70		ns
tCWL	15		20		ns
tDH	10		15		ns
tDHR	45		55		ns
tDS	0		0		ns
tPC	35		40		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCR	45		55		ns
tWCS	0		0		ns
tWP	10		15		ns

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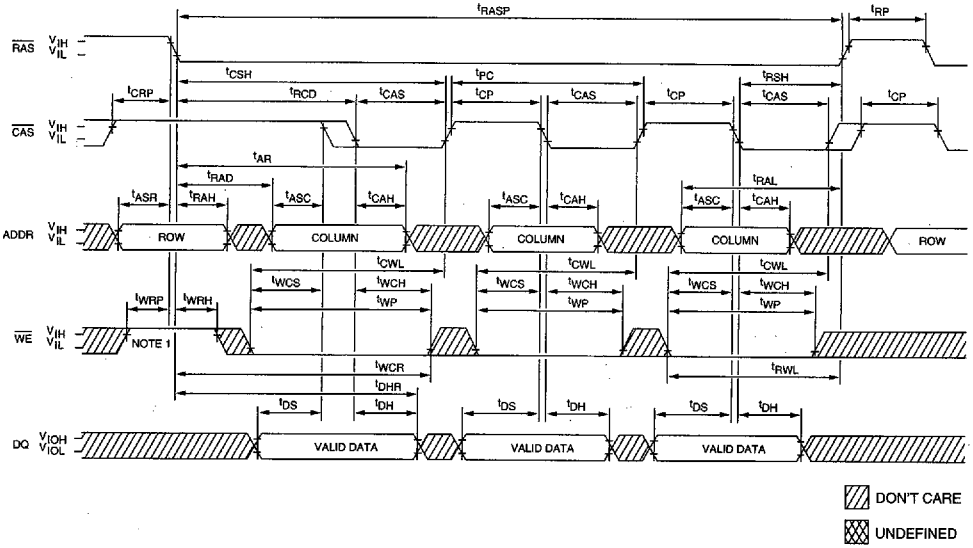
6111549 0013574 804

EDO-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		
SYM	MIN	MAX	UNITS
^{t}AR	45		ns
^{t}ASC	0		ns
^{t}ASR	0		ns
^{t}CAH	10		ns
^{t}CAS	13	10,000	ns
^{t}CP	10		ns
^{t}CRP	10		ns
^{t}CSH	50		ns
^{t}CWL	15		ns
^{t}DH	9		ns
^{t}DHR	45		ns
^{t}DS	0		ns
^{t}PC	26		ns
^{t}RAD	15	30	ns

	-6		
SYM	MIN	MAX	UNITS
^{t}RAH	10		ns
^{t}RAL	30		ns
^{t}RASP	60	100,000	ns
^{t}RCD	20	45	ns
^{t}RP	40		ns
^{t}RSH	15		ns
^{t}RWL	15		ns
^{t}WCH	10		ns
^{t}WCR	45		ns
^{t}WCS	0		ns
^{t}WP	10		ns
^{t}WRH	10		ns
^{t}WRP	10		ns

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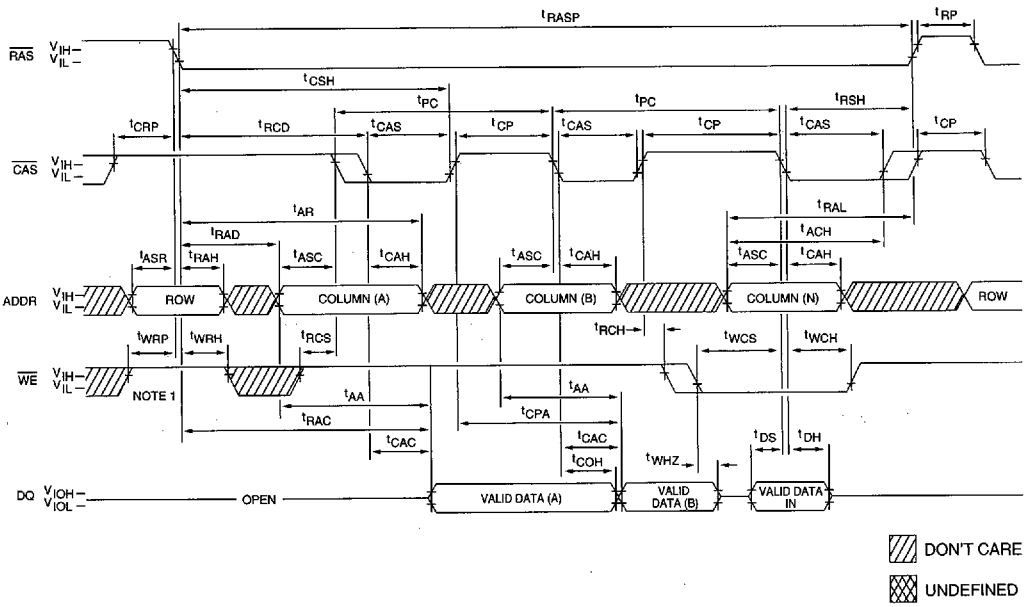
6111549 0013575 740

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		
SYM	MIN	MAX	UNITS
^{t}AA		30	ns
^{t}ACH	15		ns
^{t}AR	45		ns
^{t}ASC	0		ns
^{t}ASR	0		ns
^{t}CAC		17	ns
^{t}CAH	10		ns
^{t}CAS	13	10,000	ns
^{t}COH	5		ns
^{t}CP	10		ns
^{t}CPA		35	ns
^{t}CRP	10		ns
^{t}CSH	50		ns
^{t}DH	9		ns
^{t}DS	0		ns
^{t}PC	26		ns

	-6		
SYM	MIN	MAX	UNITS
^{t}RAC		60	ns
^{t}RAD	15	30	ns
^{t}RAH	10		ns
^{t}RAL	30		ns
^{t}RASP	60	100,000	ns
^{t}RCD	20	45	ns
^{t}RCH	0		ns
^{t}RCS	0		ns
^{t}RP	40		ns
^{t}RSH	15		ns
^{t}WCH	10		ns
^{t}WCS	0		ns
^{t}WHZ	3	15	ns
^{t}WRH	10		ns
^{t}WRP	10		ns

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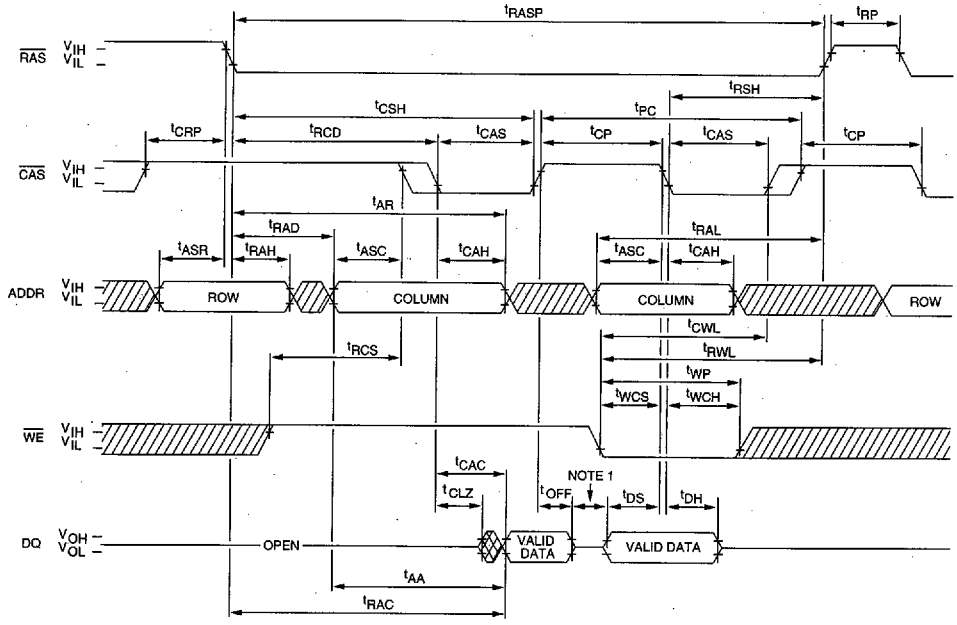
6111549 0013576 687

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	0		0		ns
tCP	10		10		ns
tCRP	10		10		ns
tCSH	60		70		ns
tCWL	15		20		ns
tDH	10		15		ns
tDS	0		0		ns
tOFF	3	15	3	20	ns

	-6		-7		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tPC	35		40		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCS	0		0		ns
tWP	10		15		ns

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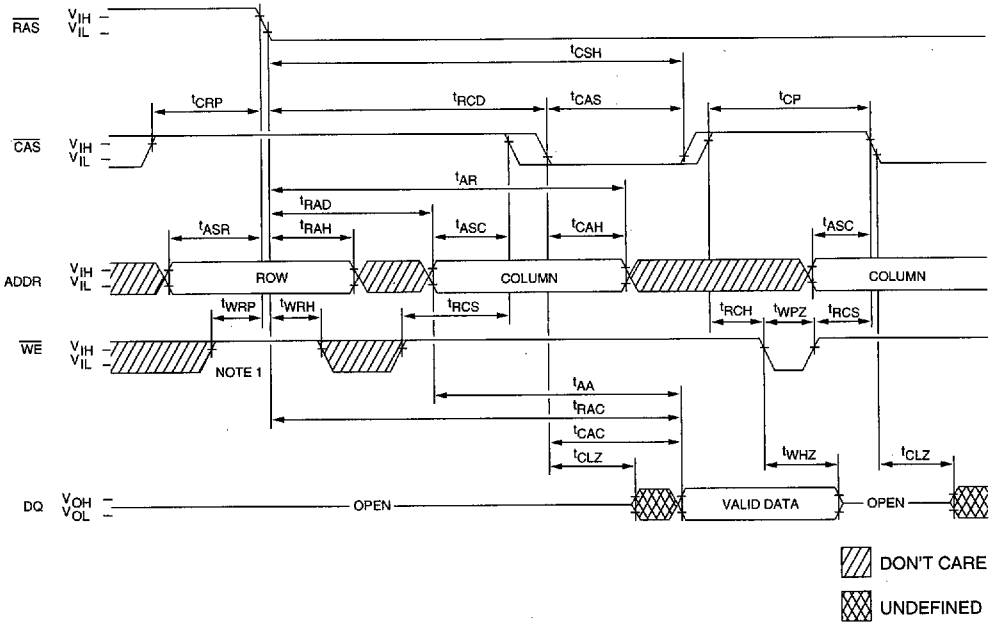
6111549 0013577 513

EDO READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		
SYM	MIN	MAX	UNITS
^{t}AA		30	ns
^{t}AR	45		ns
^{t}ASC	0		ns
^{t}ASR	0		ns
^{t}CAC		17	ns
^{t}CAH	10		ns
^{t}CAS	13	10,000	ns
^{t}CLZ	3		ns
^{t}CP	10		ns
^{t}CRP	10		ns
^{t}CSH	50		ns

	-6		
SYM	MIN	MAX	UNITS
^{t}RAC		60	ns
^{t}RAD	15	30	ns
^{t}RAH	10		ns
^{t}RCD	20	45	ns
^{t}RCH	0		ns
^{t}RCS	0		ns
^{t}WHZ	3	15	ns
^{t}WPZ	10		ns
^{t}WRH	10		ns
^{t}WRP	10		ns

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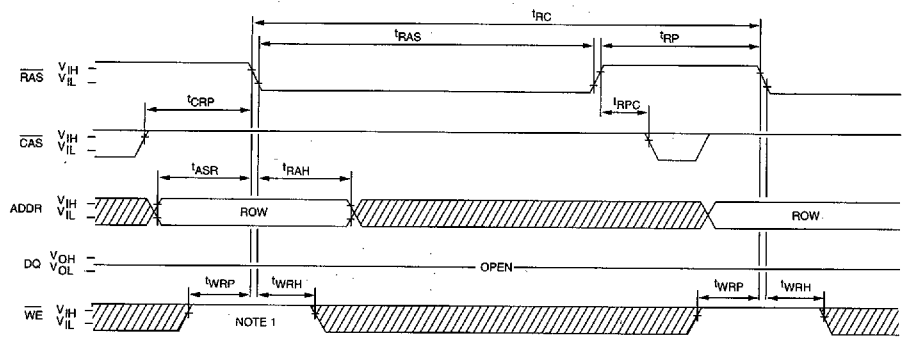
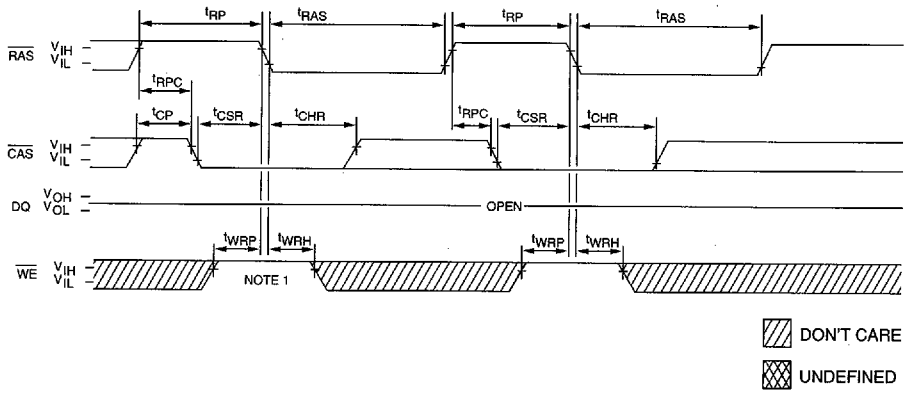
6111549 0013578 45T

RAS-ONLY REFRESH CYCLE [27]



CBR REFRESH CYCLE [29]
(Addresses = DON'T CARE)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}ASR	0		0		ns
^{t}CHR	10		10		ns
^{t}CP	10		10		ns
^{t}CRP	10		10		ns
^{t}CSR	10		10		ns
^{t}RAH	10		10		ns
^{t}RAS	60	10,000	70	10,000	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}RC	110		130		ns
^{t}RP	40		50		ns
^{t}RPC (FPM)	0		0		ns
^{t}RPC (EDO)	5		—		ns
^{t}WRH	10		10		ns
^{t}WRP	10		10		ns

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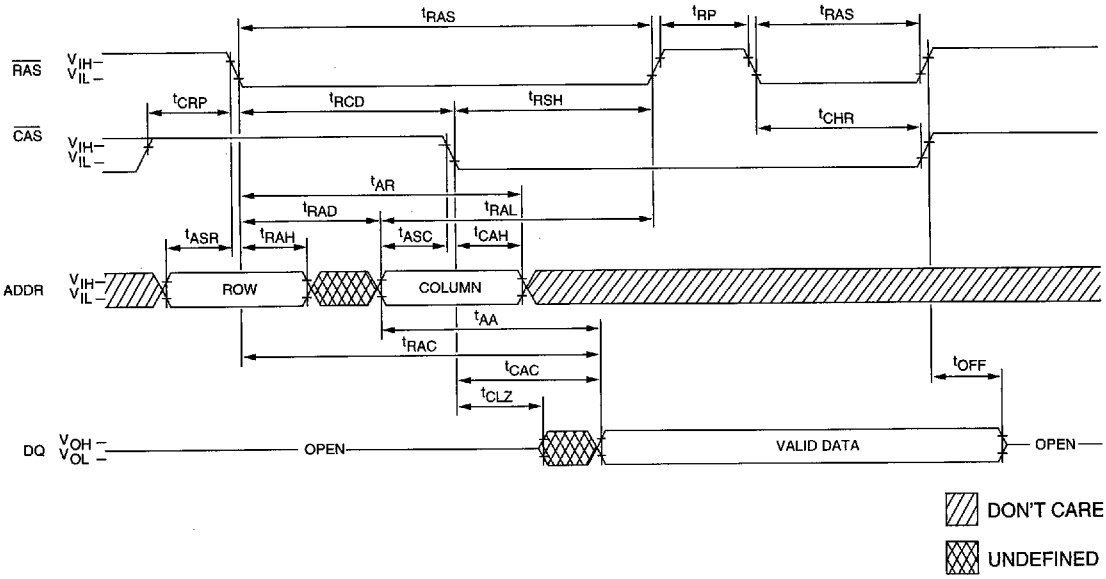
6111549 0013579 396

HIDDEN REFRESH CYCLE [20, 27]
($\overline{WE}$ = HIGH)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC (FPM)		15		20	ns
tCAC (EDO)		17		—	ns
tCAH	10		15		ns
tCHR	10		10		ns
tCLZ	3		3		ns
tCRP	10		10		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOFF	3	15	3	20	ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRCD	20	45	20	50	ns
tRP	40		50		ns
tRSH	15		20		ns

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